

Approved
CUSTOMER NO. 30430

PATENT APPLICATION
Docket No. 99-C-179D1

IN THE SPECIFICATION:

Please amend the paragraph at page 18, lines 4-18, as follows:

The first condition of the normal operating mode detects transitions of the signal level of the primary power source from a low to a high signal level. The VREF signal 104 will cross the VA3 signal 105 at the trip point of the power source switchover circuitry 103 as the supply voltage of the primary power source ramps-up. As previously discussed, the preferred embodiment sets the trip point of the power source switchover circuitry 103 to 2.5V. At the trip point of the power source switchover circuitry 103, the BCOMPOUT signal 114 transitions from a high to a low logic level indicating that the VREF signal 104 is higher than the VA3 signal 105 (i.e., the primary power source is at a normal operating level). The transition of the BCOMPOUT signal 114 causes the monitor and switchover circuitry 101 to switch from the secondary power source to the primary power source. When the BCOMPOUT signal goes high, the output of the nor gate 235, node N3, transitions from a high ~~low~~ to a low ~~high~~ logic level. Node N3 is also an input to the delay element 240. The delay element 240 may comprise a plurality of delay components (e.g., inverters) within the delay element 240 to delay the input signal by 350 nanoseconds, for example. The output of the delay element 240, node N4, transitions 350 nanoseconds after the transition of node N3.

Please amend the paragraph at page 20, lines 14-20, as follows:

Upon the power source switchover circuitry 103 detecting the signal level of the primary power source transitioning below the trip point (i.e., approximately 2.5V), the BCOMPOUT signal 114 transitions from a low to a high logic level. The LVSWITCH signal 140 remains a logic low during the slow ramp-down as the FSO signal 138 remains a high logic level. The output of the nor gate 260 transitions from a high to a low logic level, which causes the VSO signal 134 to transition to a low ~~high~~ logic level and the switch 136 to switch the secondary power source to the supply the non-volatile elements.